



Docket No.: 43890-485

PATENT

2823

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED

Re Application of

Hiroshi HAJI, et al.

Serial No.: 09/781,563

Filed: February 13, 2001

For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

APR 14 2003  
TECHNOLOGY CENTER 2800

THE COMMISSIONER FOR PATENTS AND TRADEMARKS  
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	23	20	3	\$18.00 =	\$54.00
Independent Claims	2	1	1	\$84.00 =	\$84.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
					\$0.00
Total of Above Calculations					\$138.00

Please charge my Deposit Account No. 500417 in the amount of \$138.00. An additional copy of this transmittal sheet is submitted herewith.

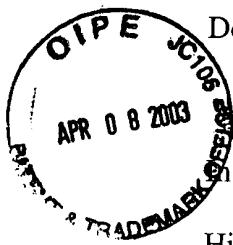
The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

*for* *Michael E. Fogarty #46,692*  
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APP. 14  
TECHNOLOGY CENTER 2800

In re Application of

Hiroshi HAJI, et al.

Serial No.: 09/781,563

Group Art Unit: 2823

Filed: February 13, 2001

Examiner: George Fourson

For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

#9/ *Answer B*  
4/15/03  
18

AMENDMENT

Commissioner for Patents  
Washington, DC 20231

Sir:

In response to the Office Action dated January 8, 2003, having a three-month shortened statutory period for response set to expire on April 8, 2003, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

IN THE CLAIMS

Please add the following new claims:

--9. A method of manufacturing a semiconductor device comprising the steps of:

forming a resin layer on a semiconductor wafer so as to form a semiconductor structure; and

cutting one of said resin layer and said semiconductor wafer along a dividing line into one of a plurality of resin layers on said semiconductor wafer and a plurality of semiconductor wafers on said resin layer, respectively.